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(54) Digital computing system with low power mode.

(57) An integrated circuit microcomputer (10) enters a low power mode in response to executing an LPSTOP instruction. Only reset events and those interrupt events having a priority level sufficiently high to pass an interrupt mask are capable of causing the termination of the low power mode. The LPSTOP instruction causes immediate data to be loaded into a status register, resetting the interrupt mask bits. The interrupt mask is then written, by means of a special bus cycle, into an interrupt mask register in a sub-system (16) within the microcomputer. This subsystem (16) then shuts down the clock signals to the remainder of the microcomputer (10), leaving only this sub-system (16) active. The active sub-system (16) performs a comparison of the priority levels of received interrupt requests to the interrupt mask during the low power mode.

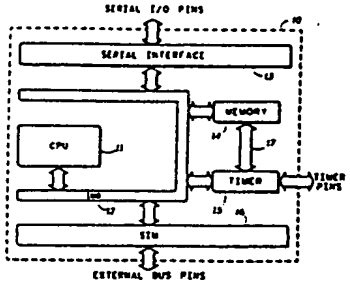

FIG.1

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FIG. 2 is a block diagram of the central processing unit of the computing system of FIG. 1;

FIG. 3 illustrates the register set of the central processing unit of FIG. 2; and

FIG. 4 is a timing diagram illustrating several bus cycles as executed by the central processing unit of FIG. 2.

Detailed Description of the Invention

The terms "assert", "assertion", "negate" and "negation" will be used to avoid confusion when dealing with a mixture of "active high" and "active low" signals. "Assert" and "assertion" are used to indicate that a signal is rendered active, or logically true. "Negate" and "negation" are used to indicate that a signal is rendered inactive, or logically false. In addition, the terms "set" and "clear" will be used when referring to the rendering of a status bit or similar apparatus into its logically true or logically false state, respectively.

FIG. 1 illustrates an integrated circuit computing system according to a particular embodiment of the present invention. A microcomputer 10 comprises a central processing unit (CPU) 11, an inter-module bus (IMB) 12, a serial communication interface 13, on-board memory 14, a timer module 15 and a system integration module (SIM) 16. Inter-module bus 12, which comprises multiple data, address and control signal lines as described in detail below, is coupled to and provides for communication between each of the other components of microcomputer 10. Serial interface 13 provides for synchronous and/or asynchronous serial data transfer between microcomputer 10 and external devices and systems by means of several serial I/O pins. Memory 14 provides storage space for software instructions and other data useful to microcomputer 10. Timer module 15 provides various timing functions such as input capture, output compare and the like by means of several timer pins and is coupled to memory 14 by means of an interface 17. SIM 16 provides an interface between IMB 12 and an external bus, the details of which are discussed below, and also provides certain system functions such as clock signal generation and distribution.

The tables which appear immediately below contain the signal definitions for all of the lines of IMB 12 and the external bus which is coupled to SIM 16. Both of these buses are parallel communication buses.

TABLE I (CONT'D)

System Reset	$\overline{\text{SYSRST}}$	Provides a "soft" reset which does not disturb system configuration data	output
SIGNAL NAME	MNE-MONIC	FUNCTION	DIRECTION
Master Reset	MSTRST	Provides a "hard" reset of everything	input
Interrupt Request Level	IRQ1 - IRQ7	Prioritized interrupt requests to the CPU	input
Autovector	AVEC	Specifies that autovector feature is to be used during an interrupt ack. cycle	input
Bus Request	BR0 - BRn	Prioritized bus mastership arbitration signals	input
Bus Lock	BLOCK	Allows bus master to retain bus	output
Test Mode	TSTMOD	Enables test mode for all devices	input
Enable IMB test lines	IMBTEST	Changes function of IRQ1-IRQ7 to test lines	input

Note that signal directions in the table above are specified with respect to CPU 11.

TABLE II

EXTERNAL BUS SIGNALS

SIGNAL NAME	MNE-MONIC	FUNCTION	DIRECTION
Address Bus	A0-A23*	24 bit address bus	input/output
Data Bus	D0-D15	16 bit data bus capable of 8 and 16 bit transfers	input/output
Function Code	FC0-FC2*	Identifies CPU state (supervisor/user) and address space of current bus cycle	input/output
Boot Chip Select	CSBOOT	Programmable chip select for boot-up	output
Bus Request	BR*	Bus Mastership Request line	input/output
Bus Grant	BG*	Bus Mastership Grant Line	output
Bus Grant Acknowledge	BGACK*	Bus Mastership Grant Acknowledge line	input/output

Test Mode Enable and Tri-State Control	$\overline{\text{TSTME}}$/TSC	Enables test mode or causes output drivers to be tri-stated	input
Clock Mode Select	MODCK	Selects source of system clock	input

The pins denoted above with an asterisk, the address pins A19-A23, the function code pins FC0-FC2, the bus request pin BR, the bus grant pin BG and the bus grant acknowledge pin BGACK, may also be used as programmable chip select pins. This feature of microcomputer 10 is not related to an understanding of the present invention. Signal directions are specified with respect to microcomputer 10.

Among the functions of SIM 16 is that of determining when a bus cycle initiated by CPU 11 is directed to a device external to microcomputer 10. If this is the case, SIM 16 executes an appropriate bus cycle on the external bus and also mediates between the internal bus cycle and the external bus cycle. In addition, SIM 16 is capable of displaying internal bus cycles which are directed at modules internal to microcomputer 10 via the external bus. This feature is useful for debugging and development purposes, among others.

FIG. 2 illustrates, in very simplified form, the internal structure of CPU 11 of FIG. 1. Fundamentally, CPU 11 comprises a micro-machine 20, an execution unit 21, a set 22 of registers and a bus interface 23. Micro-machine 20 is coupled bi-directionally to interface 23 and to execution unit 21. Registers 22 and execution unit 21 are coupled to one another by means of internal buses and the like which are not illustrated here. Execution unit 21 is also bi-directionally coupled to interface 23. Interface 23 is coupled to the address, data and control signals which comprise IMB 12.

Micro-machine 20 is responsible for determining the sequence in which instructions are to be executed, receiving the instructions from interface 23 after they have been fetched from memory (either memory module 14 or external memory), instructing interface 23 to perform instruction fetches and operand read or write cycles and decoding instructions into a plurality of control signals for use in controlling execution unit 21. As a portion of the instruction sequencing function of micro-machine 20, it performs exception processing, including the function of determining whether to acknowledge interrupt requests received via interface 23 from IMB 12. Execution unit 22 is responsible for the actual execution of the logical, arithmetic and other functions encoded in the instructions received by micro-machine 20. Registers 22 store various inputs to and results of the operations of execution unit 21. IMB interface 23 is a master-only interface to IMB 12. That is, it can initiate read and write cycles of IMB 12, and it can permit another master to initiate such cycles, but it cannot respond to either a read or a write cycle of IMB 12 which is initiated by another bus master.

Referring now to FIG. 3, register 22 of FIG. 2 are illustrated in greater detail. Registers 22 comprise 8 32-bit data registers, designated D0-D7, 7 32-bit address registers, designated A0-A6, 2 stack pointers, designated USP (for user stack pointer) and SSP (for supervisor stack pointer), respectively, a single 32-bit program counter, designated PC, a single 16-bit status register, designated SR, 2 3-bit function code registers, designated SFC (for source function code) and DFC (for destination function code), respectively, and a single 32-bit vector base register, designated VBR. The two stack pointers are alternately referred to with the designations A7 and A7', respectively.

Together, registers 22 comprise what is referred to as the programmer's model of CPU 11. The programmer's model illustrated here will be familiar to any user of microprocessors of the 68000-family of microprocessors available from Motorola, Inc. of Austin Texas.

For purposes of the present invention, only bits 8-10 of the status register SR are particularly relevant. These bits, designated I0, I1 and I2, respectively, comprise an interrupt mask. These three bits, which can encode 8 different interrupt mask settings, participate in the implementation of a prioritized interrupt recognition scheme. Basically, any interrupt source, whether internal or external, must identify its current interrupt priority level setting to CPU 11 in connection with its assertion of an interrupt request. If a requesting interrupt source has a priority level setting higher than the current mask value encoded in bits 8-10 of the status register, then the interrupt will be recognized. If the priority value is less than or equal to (except in the case of level 7 interrupts) the mask value, then the interrupt will not be recognized. Table III, below, illustrates the interrupt mask encoding scheme.

place the immediate data portion of the LPSTOP instruction into the status register SR. This has the effect of resetting the interrupt mask bits (along with the other control and condition code bits in the status register) to the values specified in the immediate data field. Next, one or more control signals are produced which cause the program counter to be incremented so as to point to the location of the next instruction to be fetched. Finally, one or more control signals are produced which cause bus interface 23 to execute a special bus cycle, the LPSTOP cycle.

The LPSTOP cycle is fundamentally a normal, internal write cycle as is described above. The LPSTOP cycle is identified as different from other write cycles by the values of the function code signals (FC0-FC2) and of certain of the address signals (A16-A19).

The function code signals identify each read or write cycle initiated by CPU 11 as being addressed to one of several possible address spaces. The various address spaces and function code signal encodings are set forth in Table IV.

TABLE IV

FUNCTION CODE ASSIGNMENTS			
FC2	FC1	FC0	ADDRESS SPACE
0	0	0	UNDEFINED
0	0	1	USER DATA
0	1	0	USER PROGRAM
0	1	1	UNDEFINED
1	0	0	UNDEFINED
1	0	1	SUPERVISOR DATA
1	1	0	SUPERVISOR PROGRAM
1	1	1	CPU

For an LPSTOP cycle the function code signals are all equal to one, making it a CPU space cycle. There are several other CPU space cycles (breakpoint and interrupt acknowledge, for example), so address lines A16-A19 are used to distinguish the CPU space cycles from one another. For the LPSTOP cycle, A19 and A18 are equal to 0 and A16 and A17 are equal to 1.

The LPSTOP cycle is one example of a special register access cycle. All special register access cycles have the function code and A16-A19 encodings described above. The lower sixteen address signals specify which special register is being accessed. In the preferred embodiment, the only special register implemented is the interrupt mask register in SIM 16, which is the destination of the LPSTOP cycle. In the general case, address signals A12-A15 identify the chip, signals A8-A11 identify the module and A0-A7 identify the special register which is the target of the special register access cycle. In the preferred embodiment, signals A0-A15 are all equal to 1 for the LPSTOP cycle.

The lower three lines of the data bus (DATA0-DATA2) are used to communicate bits 8-10 of the status register (I0-I2) during the LPSTOP cycle. SIM 16 responds to the LPSTOP cycle by storing the interrupt mask bits in its interrupt mask register.

The LPSTOP cycle is intended primarily to notify internal modules that low power mode entry is imminent and to communicate the interrupt mask bits to SIM 16. However, it is possible that devices external to microcomputer 10 may also need to be notified of the coming low power mode. Therefore, if the external bus is not under the control of an external bus master when the LPSTOP cycle is executed, the LPSTOP cycle will be executed on the external bus by SIM 16, so that external devices can prepare, if necessary, for the low power mode.

In addition to storing the interrupt mask bits, SIM 16 responds to the LPSTOP cycle by halting the IMB clock signal, CLOCK. CPU 11 and all of the other internal modules of microcomputer 10 use CLOCK as the sole source of fundamental internal timing. Thus, when CLOCK is halted, all of these modules are also halted. This greatly reduces power consumption. SIM 16 continues to generate clock signals for its own use, and so remains "awake" during the low power mode. The externally-supplied clock signal, CLK, may or may not be halted during the low power mode, depending on the state of a control bit which is set within SIM 16 under control of CPU 11.

Events which can terminate the low power mode are resets (an external device holding the $\overline{\text{RESET}}$ pin low for a predetermined period of time) and interrupts which have a priority level sufficiently high not to be

a communication bus (12) coupled to the central processing unit (10); and
clock signal generation logic (16) connected to the central processing unit to provide the clock signal thereto;
wherein the improvement comprises:
the first means (21) responds to a particular one of the instructions by placing signals representing the interrupt mask on the communication bus (12) and by causing the clock signal generation logic (16) to cease providing the clock signal to the central processing unit (11).

2. A digital computing system (10) according to claim 1 wherein the improvement further comprises:
first logic means (16) coupled to the communication bus for storing the signals representing the interrupt mask;
second logic means (16) coupled to the first logic means and being active only if the clock signal generation logic is not providing the clock signal to the central processing unit for responding to an interrupt request signal by comparing a priority level of the interrupt request signal to the contents of the first logic means (16); third logic means (16) for selectively causing the clock signal generation logic to resume providing the clock signal to the central processing unit dependent on a result of the comparison performed by the second logic means; and
the clock signal generation logic continuously provides a clock signal to the first, second and third logic means.

3. A digital computing system according to claim 2 wherein the improvement further comprises:
the first means (21) further responds to the particular one of the instructions by storing in the register means (22) an immediate bit field of the particular one of the instructions.

4. An integrated circuit digital computing system (10) comprising an inter-module communication bus (12);
a central processing unit (11) comprising:
first interrupt mask means (22) for storing an interrupt mask;
a bus controller (23) coupled to the inter-module communication bus (12); and
first interrupt means (20) for selectively responding to an interrupt request received via the bus controller (23) from the inter-module communication bus (12) dependent on a comparison between a priority level of the interrupt request and the interrupt mask; and
execution means (21) for executing instructions, the execution means is responsive to a particular instruction by causing the bus controller (23) to place predetermined signals and the interrupt mask on the inter-module communication bus (12);
an integration module (16) coupled to the inter-module communication bus (12) comprising:
second interrupt mask means (16) for storing, in response to the the receipt of the predetermined signals from the inter-module communication bus (12), the interrupt mask; and
clock signal generation means (16) for providing, via the inter-module communication bus (12), a clock signal to the central processing unit and for ceasing to provide the clock signal to the central processing unit in response to the receipt of the predetermined signals and interrupt mask from the inter-module communication bus (12).

5. An integrated circuit digital computing system (10) according to claim 4 wherein the integration module (16) further comprises:
second interrupt means (16) for selectively responding to an interrupt request dependent on a comparison between a priority level of the interrupt request and the interrupt mask stored in the second interrupt mask means (16); and
the clock signal generation means (16) is responsive to the second interrupt means to resume providing the clock signal to the central processing unit.

6.An integrated circuit digital computing system according to claim 4 wherein the integration module further comprises:
means (16) for coupling the system to an external bus, the means for coupling being responsive to receipt of the predetermined signals and interrupt mask to place the predetermined signals and the interrupt mask on the external bus.

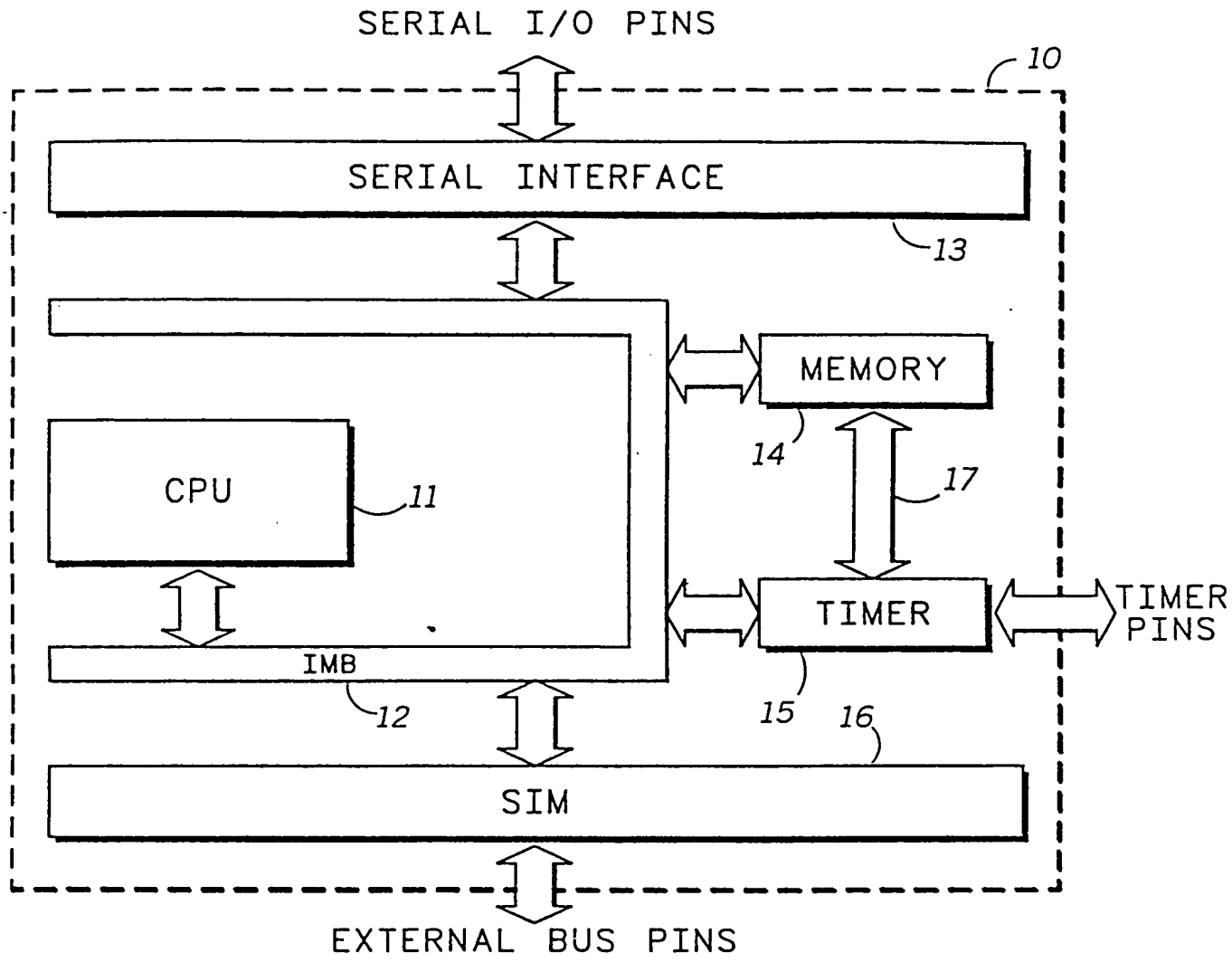
SERIAL I/O PINS
10
SERIAL INTERFACE
13
MEMORY
14
17
CPU
11
TIMER
TIMER PINS
IMB
12
15
16
SIM
EXTERNAL BUS PINS

FIG.1

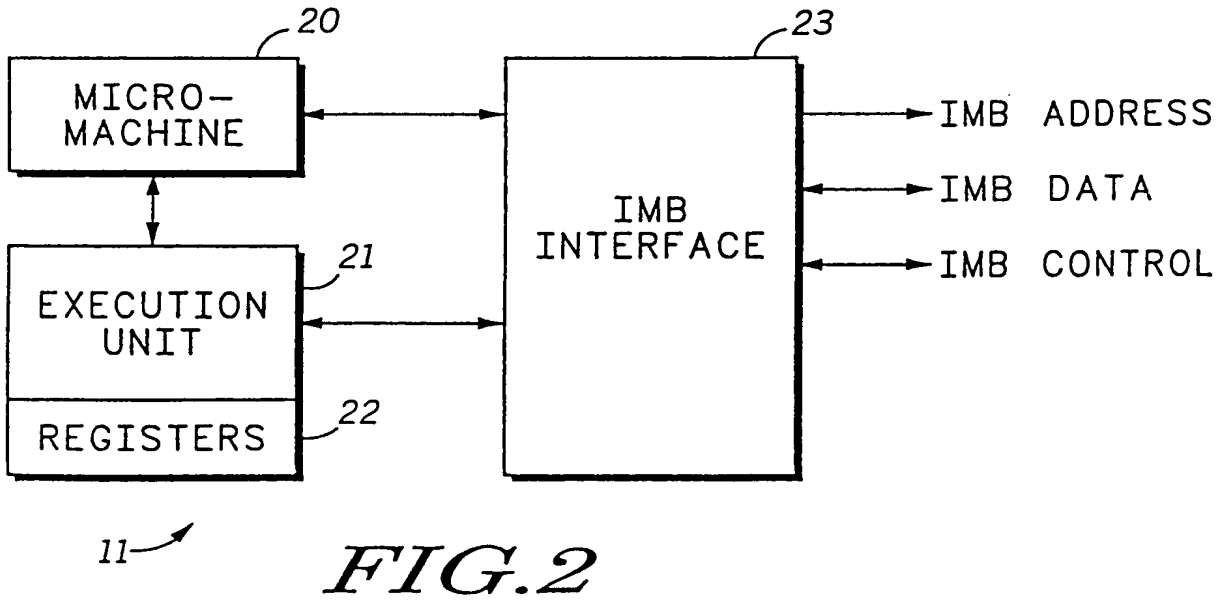
20
23
MICRO-MACHINE
IMB INTERFACE
IMB ADDRESS
IMB DATA
IMB CONTROL
EXECUTION UNIT
21
REGISTERS
22
11

FIG.2

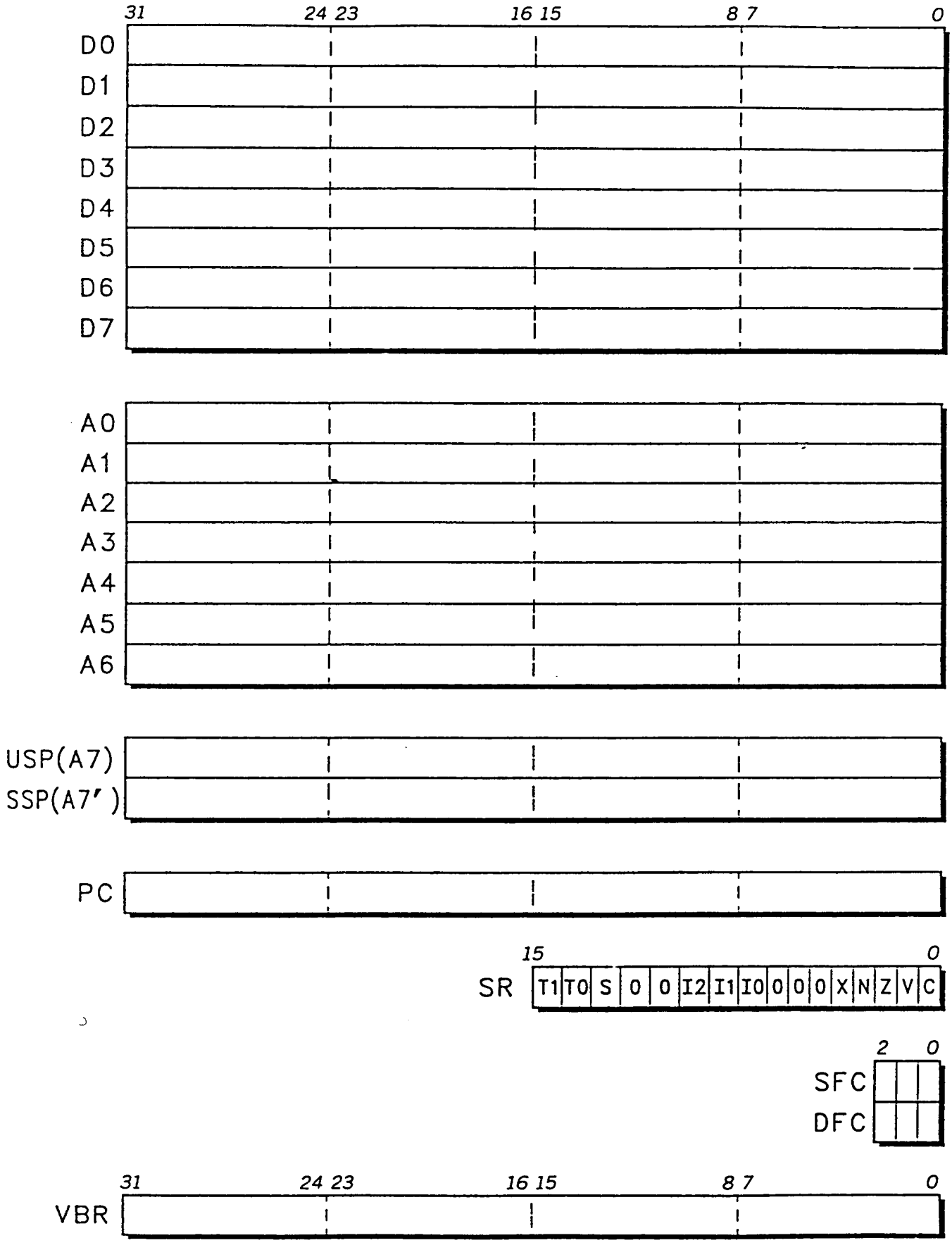
31
24 23
16 15
8 7
0
D0
D1
D2
D3
D4
D5
D6
D7
A0
A1
A2
A3
A4
A5
A6
USP(A7)
SSP(A7')
PC
15
0
SR
T1 T0 S 0 0 I2 I1 I0 0 0 0 X N Z V C
2
0
SFC
DFC
31
24 23
16 15
8 7
0
VBR

FIG.3

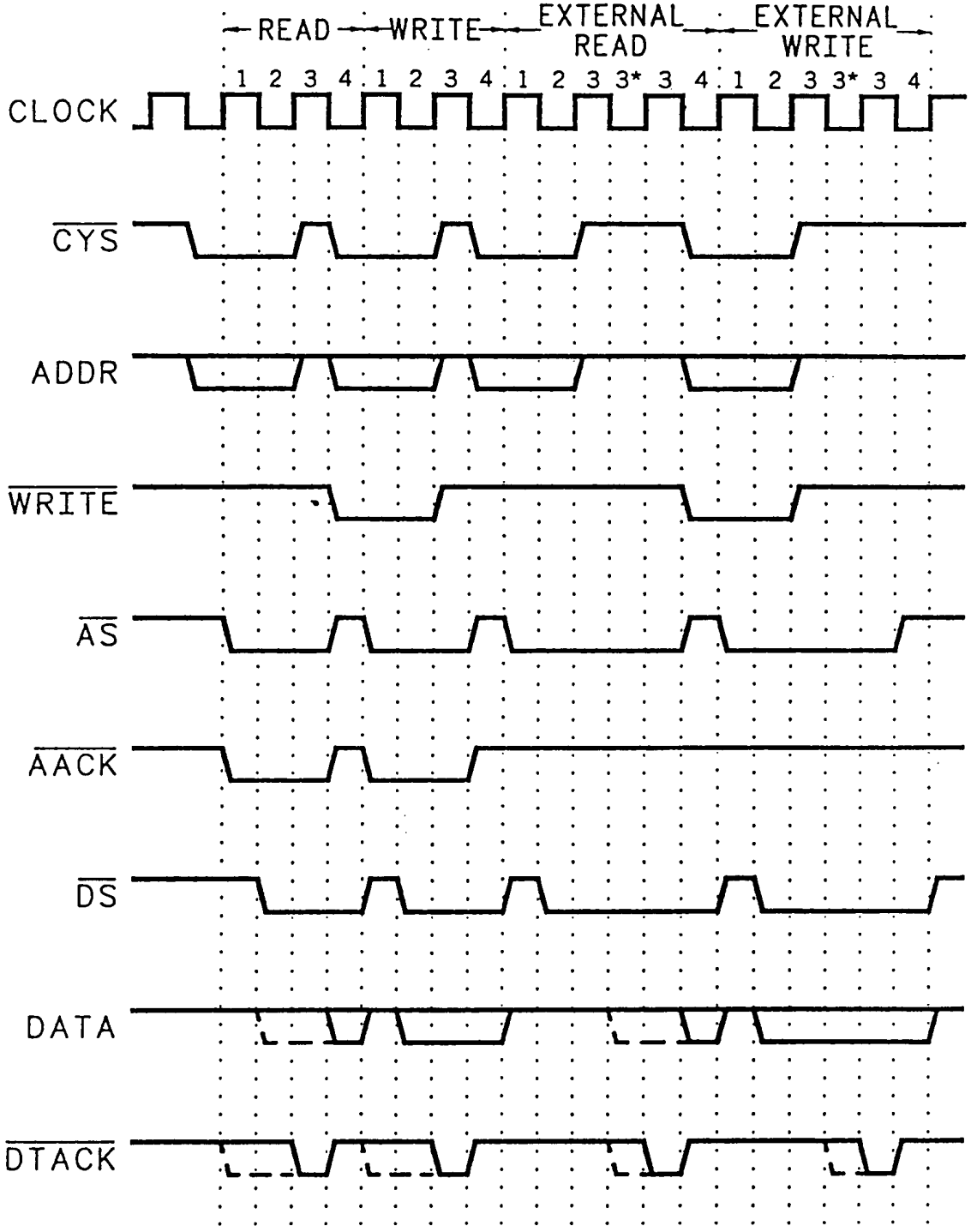
READ
WRITE
EXTERNAL READ
EXTERNAL WRITE
1 2 3 4 1 2 3 4 1 2 3 3* 3 4 1 2 3 3* 3 4
CLOCK
CYS
ADDR
WRITE
AS
AACK
DS
DATA
DTACK

FIG.4

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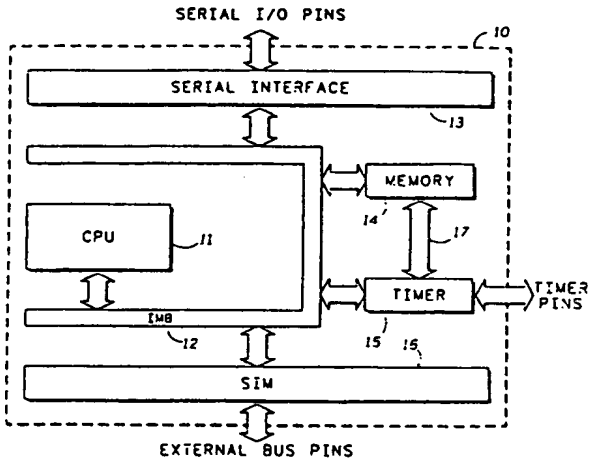

FIG.1

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European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 89 12 0284

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. 5)
A	EP-A-0 050 844 (HITACHI LTD) * Page 9, line 6 - page 10, line 18; page 11, lines 3-19 *	1,2	G 06 F 1/32
D,A	US-A-4 748 559 (P.S. SMITH et al.) * Whole document *	1,2	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

G 06 F 1
G 06 F 13

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	06-09-1990	ALONSO Y GOICOLEA L.

CATEGORY OF CITED DOCUMENTS

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